Title: 60 GHz CMOS Power Amplifiers

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Duration: 90 minutes

The availability of an unlicensed 7 GHz bandwidth around 60 GHz offers great potential for establishment of high-data-rate short-range wireless communication links. Although previously left unutilized, recent advances in electronics enable the development of wireless transceivers at millimeter-wave frequencies. Despite offering a large bandwidth, the high signal attenuation caused by oxygen absorption in 60 GHz band requires the wireless transmitters to transmit signals with power as large as 27 dBm, so the receivers can detect the greatly attenuated signals. Therefore, the design of power amplifier capable of generating such large output powers proves to be a major challenge in the development of 60 GHz wireless transceivers, especially if CMOS technology is chosen for implementation of fully integrated 60 GHz wireless systems.

This workshop presentation focused on the design and implementation of 60 GHz power amplifiers in CMOS technology. Although CMOS offers a higher level of integration and lower fabrication cost compared to high-speed compound semiconductor technologies, low supply and breakdown voltages as well as operation near cutoff frequencies of MOSFETs make the design of power amplifier extremely challenging. Optimization of the gain/power performance of CMOS power amplifiers operating at millimeter wave frequencies requires novelty in the design of active/passive structures. On-chip passive transformers are widely used for combining the output power of individual power amplifier stages as they can simultaneously perform impedance matching, AC coupling, DC biasing, and the power combination. Design of high efficiency transformers for combining the output power of amplifiers of more than two stages is a challenging part of the implementation which requires novelty in modeling and layout optimization techniques. In this presentation, an overview on the technological advances and the challenges in millimeter wave CMOS power amplifiers is presented comparing previously reported active/passive power combination techniques.

Design of most recently published 60 GHz PA microchips is discussed. Characterization and optimization of passive devices is performed using extensive finite-element electromagnetic (EM) simulations. Power MOSFETs are fabricated and characterized at mmW frequencies. Novel Circuit topologies and power combining architectures are utilized to increase the gain, bandwidth, efficiency and output power of the fabricated PAs. Circuit design methods for proposed topologies in 65nm TSMC CMOS technology are presented. Finally, measurement methods using advanced mmW test setups are described.